

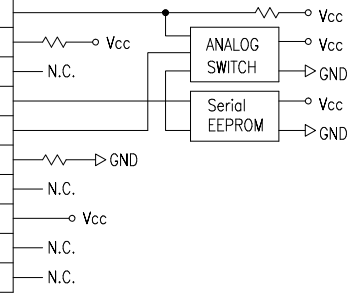
REVISION AND CHANGE EFFECTIVITY DATE				
LTR.	ECN	DESCRIPTION	DATE	APP'D.

Wiring Diagram

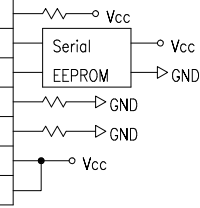
High Speed Signal					
P0(4x-Pluggable-QSFP+)			SFP+		
Pad	Signal		Pad	Signal	
36	TX1p		13	RX+	P1
37	TX1n		12	RX-	
18	RX1n		19	TX-	P2
17	RX1p		18	TX+	
GND Group	GND		GND Group	GND	
03	TX2p		13	RX+	P3
02	TX2n		12	RX-	
21	RX2n		19	TX-	P4
22	RX2p		18	TX+	
GND Group	GND		GND Group	GND	
33	TX3p		13	RX+	P1~P4
34	TX3n		12	RX-	
15	RX3n		19	TX-	GND Group
14	RX3p		18	TX+	
GND Group	GND		GND Group	GND	
06	TX4p		13	RX+	P1~P4 GND Group:
05	TX4n		12	RX-	
24	RX4n		19	TX-	11,14,17,20
25	RX4p		18	TX+	
GND Group	GND		GND Group	GND	
GND Group: 01,04,07,13,16,19 20,23,26,32,35,38			P1~P4 GND Group: 01,02,06,08,10, 11,14,17,20		
Connector Shell			P1~P4 Connector Shell		

*DC Blocking Caps on P0-P4 Rx Side.

Low Speed Signal & Power	
P0(4x-Pluggable-QSFP+)	
Pad	SIGNAL
08	ModSelL
09	ResetL
10	VccRx
11	SCL
12	SDA
27	ModPrsL
28	IntL
29	VccTx
30	Vcc1
31	LPMode



Low Speed Signal & Power	
P1-P4(SFP+)	
Pad	Signal
03	TX_Disable
04	SDA
05	SCL
07	RS0
09	RS1
15	VCCR
16	VCCT



DO NOT SCALE DRAWING.



EXPERIMENTAL NO:		DIVISION ASSIGNED: dataMATE Division	
TOLERANCES UNLESS OTHERWISE SPECIFIED		MATERIAL: SEE NOTES	
METRIC INCHES		DRAWN BY: A. PIRILLIS DATE: 11/26/12	
X ± .26 FRACTION DEC. XX ± .010		CHECKED BY: B. SKEPNEK DATE: 11/26/12	
XX ± .13 ANGLES ± .005		ENGR. APPROVAL: J. LLORENS DATE: 11/26/12	
TOOLING DWG <input type="checkbox"/>		APPROVED BY: A. CHIAPPETTA DATE: 11/26/12	
PART DWG <input type="checkbox"/>		PART NO. CLASSIFICATION:	
BREAK SHARP EDGES REMOVE ALL BURRS		SIZE C CODE IDENT. DWG. NUMBER Rev.	
THE INFORMATION DISCLOSED IN THIS DOCUMENT IS PROPRIETARY TO METHOD ELECTRONICS, INC. AND MAY NOT BE USED FOR MANUFACTURE OR ANY OTHER PURPOSE WITHOUT THE WRITTEN CONSENT OF METHOD. DETAILS SUBJECT TO CHANGE AS THEY MAY AFFECT WITH RESPECT TO PRODUCT PERFORMANCE.		DM-3B3-XXX	
SCALE:		SHT. 2 OF 2	